UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/835,170	04/13/2001	Spencer Gold	P5213/SMQ-041	4882

959 7590 01/03/2006

LAHIVE & COCKFIELD, LLP.
28 STATE STREET
BOSTON, MA 02109

EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/835,170	GOLD, SPENCER	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 24-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. Applicant's arguments/amendments with respect to previously presented claims 1-29 filed November 17, 2005 have been fully considered but are moot in view of new grounds of rejection.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6 and 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (USPN 5854801).

As per claims 1 and 24, Yamada et al. (herein after: Yamada) substantially teaches (title, abstract and Figure 1) a method and apparatus for generating patterns for SDRAM memory. A test pattern is generated for the SDRAM by having a specific wrap conversion circuit or an address conversion method. The wrap conversion circuit is provided to receive two kinds of data from a pattern generator and converts the data through a predetermined logic circuit information.

The test pattern generation method for the SDRAM is carried out by inputting the column address data Y0-Y2 and the wrap address data Z0-Z2, and by generating output data which has been converted by a predetermined logic equation. The test pattern generation apparatus and method can also include an address inversion scramble for the converted output. Furthermore, Yamada teaches (Figure 1) the wrap address conversion circuit 40 is provided at an output of a pattern generator 10. For the wrap address conversion circuit 40, data (Y0-Y8) corresponding to the bit length of the column address of the SDRAM is provided from the pattern generator 10. At the same time, data (Z0-Z2) corresponding to the bit length of the wrap address of the SDRAM is provided to the wrap address conversion circuit 40 from the pattern generator 10. Yamada also teaches (col. 4, lines 25-65) the address inversion scramble is used for converting the address between the logical address and the physical address of the device under test. This is a function to convert the address because the chip alignment within the device to be tested is freely designed and determined to meet the physical and operational conditions of the device for each kind of devices and such an alignment does not match the logical address given at the outside of the device. Thus, the address inversion scramble is a function necessary to perform failure analysis with respect to the internal operation of the device under test.

Yamada does not explicitly teach an integrated circuit as stated in the present application.

However, the Examiner would like to point out that arranging elements to be on a single integrated circuit does not render the claims of the present application patentably distinct over the prior art of record. See ***In re Larson 144 USPQ 347 (CCPA 1965)***. One of ordinary skill in the art at the time the invention was made would have been motivated to integrated the teachings of Yamada onto a single networked circuit. This would have been obvious to one or ordinary

skill in the art because one of ordinary skill in the art would have recognized that by including all the essential elements onto a single integrated circuit would have made testing of the circuit more versatile and is well-known in the art.

As per claims 2-4 and 25-27, Yamada et al. (herein after: Yamada) substantially teaches, in view of above rejections, a conversion circuit as shown in Figure 1.

Yamada does not explicitly teach the conversion circuit to comprise of a ROM, RAM or EEPROM as stated in the present application.

However, Yamada teaches (col. 2, lines 10-63) a test pattern generation apparatus is provided to effectively test an SDRAM. The pattern generation apparatus includes a-wrap address conversion means which is provided with two (2) kinds of data (Y0-Y2) and (Z0-Z2) from a pattern generator and outputs converted addresses which have been converted based on a predetermined logic circuit information in the conversion means. The Examiner would like to point out that the conversion circuit inherently has to have temporarily storage device, for example a RAM, which is a type of storage memory that can be used while operating. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a RAM, ROM or EEPROM within the conversion circuit of Yamada. This modification would have been obvious to one of ordinary skill because one of ordinary skill would have recognized that the use of EEPROM, RAM or ROM allows the electronic device to detect nonfunctional memory cell locations.

As per claims 5-6 and 28-29, Yamada et al. (herein after: Yamada) substantially teaches, in view of above rejections, the address inversion scramble is used for converting the address between the logical address and the physical address of the device under test. This is a function

to convert the address because the chip alignment within the device to be tested is freely designed and determined to meet the physical and operational conditions of the device for each kind of devices and such an alignment does not match the logical address given at the outside of the device. Thus, the address inversion scramble is a function necessary to perform failure analysis with respect to the internal operation of the device under test. Further, the output of the wrap conversion circuit 40 can be given to a failure analysis apparatus.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
December 26, 2005

ALBERT DECADY
SUPERVISORY PATENT EXAMINER